

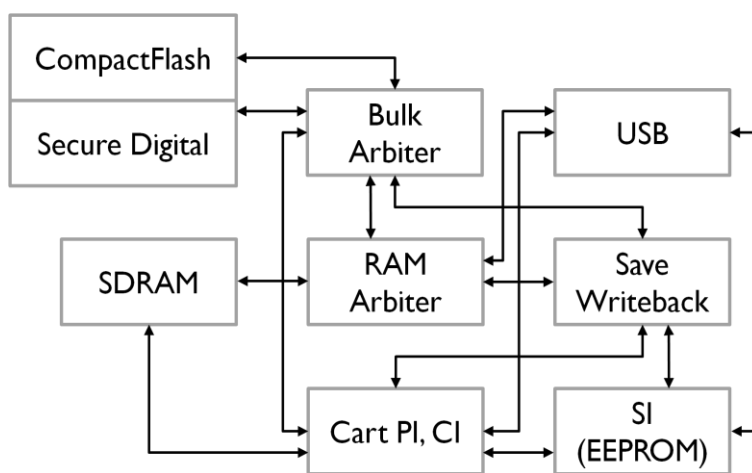
HARDWARE USAGE GUIDE

(FIRMWARES 2.XX)

OVERVIEW

All of the 64drive's functionality is facilitated by the onboard FPGA. Automatically configured on every power-on, the FPGA's job is to coordinate communication between components on the 64drive circuit board such as SDRAM, USB, and the PI bus. In addition to emulating the N64's cartridge bus protocol, the FPGA also emulates all N64 save types.

BLOCK DIAGRAM



MODES OF OPERATION

The 64drive can be operated in one of two modes at a time:

	Bootloader	CIC Emu	Save Writeback	Save Emulation	CI Access	USB
MENU MODE	✓	✓	✓	✓	✓	✓
DEV MODE				✓	✓	✓

MENU MODE

Upon power-up in an N64 console, the 64drive boots into menu mode. In this mode, the N64 boots from the bootloader, which then locates MENU.BIN from the memory card, transfers to cart ROM and runs it.

DEV MODE

When the user plugs in a USB cable the 64drive switches to dev mode. This mode most closely resembles a real, single-image cartridge. It is intended that the user uploads an image to SDRAM using PC-side software prior to booting the N64.

While save chips may be emulated, any changes in their data will not be flushed back to the memory. You must manually upload and download the contents of these save memory banks with the companion PC software.

CI (CARTRIDGE INTERFACE)

OVERVIEW

The 'CI' interface is a small range of memory in the upper area of the PI address space that contains registers and some block memory associated with the 64drive hardware.

REGISTERS

ADDRESS	SIZE	FUNCTION	READ	WRITE
0x1800 0000	512 bytes	Buffer (256 words)	✓	✓
0x1800 0200	16 bits	Status Register	✓	
0x1800 0208	32 bits	Command Register		✓
0x1800 0210	32 bits	LBA Register		✓
0x1800 0218	32 bits	Length Register	✓	✓
0x1800 02E8	32 bits	SDRAM Size (bytes)	✓	
0x1800 02EC	32 bits	Hardware Magic	✓	
0x1800 02F0	32 bits	Hardware Variant	✓	
0x1800 02F4	32 bits	Persistent Variable Storage	✓	✓
0x1800 02F8	16 bits	Button Register	✓	
0x1800 02FA	16 bits	Upgrade Module Status	✓	
0x1800 02FC	16 bits	Revision Register	✓	
0x1800 1000	2048 bytes	EEPROM contents (1024 words)	✓	✓
0x1800 1800	1024 bytes	Save Writeback LBA List (256 dwords)	✓	✓

TO PERFORM A COMMAND:

1. Check the status register to make sure CI is idle
2. Write all necessary parameters to the appropriate registers
3. Write the command code to the command register
4. Poll status for completion (same as step 1)

STATUS REGISTER TABLE

Bit Range	[15:12]	[11:8]	[7:4]	[3:0]
Function	0x0 – CI Idle 0x1 – CI Busy	Reserved	Reserved	Reserved

CI COMMAND TABLE

COMMAND	ID	PARAMETERS
READ SECTOR INTO BUFFER	0x01	LBA
READ MULTIPLE SECTORS TO SDRAM	0x03	LBA, RAMADDR, NUM_SEC
WRITE BUFFER INTO SECTOR	0x10	LBA
WRITE MULTIPLE SECTORS FROM SDRAM	0x13	LBA, RAMADDR, NUM_SEC
[RESERVED]	0x30	-
[RESERVED]	0x31	-
SET SAVE TYPE	0xD0	SAVE_TYPE
DISABLE SAVE WRITEBACK	0xD1	-
ENABLE SAVE WRITEBACK	0xD2	-
DISABLE BYTESWAP ON LOAD	0xE0	-
ENABLE BYTESWAP ON LOAD	0xE1	-
ENABLE CARTROM WRITES	0xF0	-
DISABLE CARTROM WRITES	0xF1	-
START FIRMWARE UPGRADE	0xFA	MAGIC
SET CF PULSE WIDTH	0xFD	NUM_CYCLES

All reserved bitfields should be masked off and ignored, as they may be used in future versions for additional functionality.

COMMAND LISTING

MEMORY CARD ACCESS

When power is first applied, the 64drive tests to see if a CF card is inserted. If so, it will always use it until power is lost. If no CF was detected, SD will be used instead. SD is only initialized once upon powerup, so hot-swapping is not supported.

READ SECTOR INTO BUFFER

Reads a single sector from the memory card into the main buffer.

0x1800 0210 [LBA REG]	LBA (sector number)
-----------------------	---------------------

READ MULTIPLE SECTORS TO SDRAM

Copies any number of sectors from the memory card to an address in SDRAM.

0x1800 0210 [LBA REG]	LBA (sector number)
0x1800 0218 [LENGTH REG]	Number of sectors
0x1800 0004 [in buffer]	SDRAM address (0x0 - 0x1FFFFFFF)

WRITE SECTOR FROM BUFFER

Writes the FPGA's 512 byte buffer to the memory card sector specified in the LBA register.

0x1800 0210 [LBA REG]	LBA (sector number)
-----------------------	---------------------

WRITE MULTIPLE SECTORS FROM SDRAM

Copies any number of sectors to the memory card from an address in SDRAM.

0x1800 0210 [LBA REG]	LBA (sector number)
0x1800 0218 [LENGTH REG]	Number of sectors
0x1800 0004	SDRAM address (0x0 - 0x1FFFFFFF)

SET CF PULSE WIDTH

Sets the pulse width (in number of clock cycles) of OE and WE for the CompactFlash interface. Currently the core FPGA logic runs at 50MHz so each cycle period is 20ns. Setting this value too low may cause data corruption. The bootloader optimizes this number on bootup to get faster transfers.

0x1800 0000	Clock cycles (Default: 10 → 200ns)
-------------	------------------------------------

DISABLE BYTESWAP ON LOAD

Sets normal byte ordering (Z64).

ENABLE BYTESWAP ON LOAD

Causes all data transferred directly from the memory card to SDRAM to be byteswapped, for loading V64 format images. This has no effect on copying from the buffer to SDRAM. Transfers (writes) back to memory card are not affected. The default is `DISABLED`.

SAVE MEMORY EMULATION

SET SAVE TYPE

The 64drive supports all save types found in commercial software images. This command sets the type of save that the FPGA should emulate.

Note: Due to hardware limitations in hardware variant A, the Pokemon Stadium 2 images are handled specifically.

0x1800 0000

Save type:

0 = None

1 = EEPROM 4Kbit

2 = EEPROM 16Kbit

3 = SRAM 256Kbit

4 = FlashRAM 1Mbit

5 = SRAM 768Kbit (for Dezaemon 3D)

6 = FlashRAM 1Mbit (for Pokemon Stadium 2)

⚠ WARNING

Do not enable saving until the LBA writeback list is populated. The LBAs are zero upon powerup. If the SWB (Save Writeback module) finds a zero-value LBA, it will cancel the operation to prevent FAT corruption. However, it's best to not put this to the test.

DISABLE SAVE WRITEBACK

Inhibits the Save Writeback module (SWB), preventing any save persistence. This is automatically set upon USB cable insertion (**USB MODE**).

ENABLE SAVE WRITEBACK

Default mode when booting in menu mode. Throughout gameplay in **MENU MODE**, periodically flushes new savegame data back to the memory card via the Save Writeback LBA list.

MISCELLANEOUS

ENABLE CARTROM WRITES

Normally, reads from cartridge space (0x1000 0000-0x1400 0000) are mapped to SDRAM, while writes to this space are ignored. This command allows writes to this range to fall through to SDRAM. Necessary for setting up a multi-block DMA from RAM to memory card. The default is `DISABLED`.

DISABLE CARTROM WRITES

Locks cartridge ROM (SDRAM) against direct modification by the N64. This is the default state on boot in both menu and dev mode.

For basic communication between some custom PC software and the N64 running homebrew, enabling ROM writes and treating part of it as a dual-access scratchpad should work until proper USB FIFO access is supported in the next firmware.

START FIRMWARE UPGRADE

Initiates the on-chip firmware flashing engine. Special firmware blob must be written to SDRAM in preparation. The upgrade module will read the blob and perform several verifications.

If all checks pass, it flashes the configuration ROM with the new data.

If there is any failure, the module will stop and lock itself out until the next power cycle.

The upgrade module can be kickstarted either from CI or the USB interface. In each case, the same status codes are read out to check on the upgrade's progress.

0x1800 0000	Magic (0x55504752)
-------------	--------------------

ADDITIONAL REGISTERS

In addition to the registers used for commands, there are several other registers that contain information about the device.

SDRAM SIZE

The total number in bytes of SDRAM on the device – 67108864 bytes (64MByte).

DEVICE MAGIC

A four-character ASCII string with the product series code – “UDEV”

DEVICE VARIANT

An ASCII variant letter identifying the specific variation of the device. Existing hardware revisions return 0x00004100 (“A “) [letter A and an ASCII null terminator]. Future revisions may not contain a null terminator, as in the case of a two-letter variant.

REVISION (VERSION) REGISTER

The lower 16 bits of this register contain the FPGA configuration revision number. The top 16 bits are unspecified, so the value returned from this register should be AND'd with 0xFFFF. For example, a value of decimal “203” means version 2.03. This information is displayed in the About tab of the menu.

PERSISTENT VARIABLE STORAGE

This register is 4 bytes of storage that can be used for any purpose. The bootloader writes its version number to this register so that the menu can read it later on, as well as support for Reset-To-Game.

BUTTON REGISTER

The state of the hardware button. The button input is not filtered, so debouncing should be performed in software. Nonzero when depressed, zero otherwise.

UPGRADE STATUS REGISTER

The current response from the Upgrade Module (UPG).

Bit Range	[15]	[14:4]	[3:0]
Function	0x0 – Not valid 0x1 – Status Valid	Reserved	0x1 – Ready 0x2 – Verifying 0x3-0x6 – Erasing 0x7-0xA – Writing 0xC – Success 0xD – General fail 0xE – Bad variant 0xF – Verify failed

EEPROM CONTENTS

A 2048-byte (1024 word) buffer that stores the contents of the EEPROM save chip being emulated. The menu writes to this when loading an image if that image has EEPROM save data associated with it. During gameplay, when the game writes save data it will be saved in this buffer.

If the **SET SAVE TYPE** command is executed with the parameter '1', the valid size is 512 bytes. If it is executed with '2', the valid size is 2048 bytes.

WARNING

This memory is muxed three ways among USB, CI, and the Save Writeback module. Any module attempting to monopolize access does so at the expense of the others.

SAVE WRITEBACK LBA LIST

A 1024-byte (256 LBA) buffer that stores a list of LBAs occupied by the image's save file. The LBAs are stored as 32 bits each, although internally 27 bit LBA addressing is used.

Upon a save writeback event (usually triggered by the N64 modifying the save memory followed by a timeout) the save data is flushed back to the memory card by writing the save data to these sectors. Such an event can be noticed by carefully watching the status LED on the circuit board inside the case. It will flash in a regular pattern for about half a second.

In 1.xx series firmware this only happened due to Reset/NMI firing. In 2.xx this can occur at any time. The writeback state machine performs writes to contiguous runs of LBAs in a single pass so that a non-fragmented file will be written in 1 pass. If the save file is fragmented, it will be written in multiple runs.

USB INTERFACE

OVERVIEW

This section is under further development.

Refer to the USB Loader source code for a starting point. As of firmware 2.00 there is no user mode FIFO available from CI space, but it is planned for future versions. For now the cartridge ROM can be written and treated like a dual-port scratchpad.

Suggestions are welcome.

END OF DOCUMENT

REVISION INFORMATION

November 4, 2014	First internal draft
January 7, 2015	Current internal revision

COPYRIGHT INFORMATION

© 2011-2015 Marshall H / Retroactive

<http://64drive.retroactive.be/>

"Nintendo" is a registered trademark of Nintendo of America Inc.

Nintendo 64 is a registered trademark of Nintendo Company, Limited

This product is not endorsed or supported by Nintendo. Use the device at your own risk.

To submit any inaccuracies or inconsistencies in this document, please e-mail support at the above web address.